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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,012	10/14/2003	Timothy J. Dalton	YOR920030336US1 (16898)	4288

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SCULLY SCOTT MURPHY & PRESSER, PC
400 GARDEN CITY PLAZA
SUITE 300
GARDEN CITY, NY 11530

EXAMINER	
ORTIZ, EDGARDO	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,012	DALTON ET AL.	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims contains the limitation "wherein said sidewalls are not substantially altered either chemically or physically", however the metes and bounds of the claimed language are unclear since it is not clear what Applicant regards as "*not substantially altered*".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gabriel et al. (U.S. Patent No. 6,472,231) in view of Wang et al. (U.S. Patent No. 6,140,706). With regard to Claim 1, as best the examiner is able to ascertain the claimed invention, Gabriel discloses on figure 7 an interconnect structure (column 5, lines 54-56) comprising:

a semiconductor substrate (10) comprising one or more device regions (column 5, lines 62-63); and

one or more interconnect levels located atop the semiconductor substrate, said one or more interconnect levels comprising a patterned organosilicate dielectric layer (14) (column 5, lines 66-67) having sidewalls.

However, Gabriel fails to disclose the claimed sidewalls of the patterned organosilicate dielectric layer not being substantially altered either chemically or physically. However, Wang discloses on figure 1B a semiconductor device including a metal interconnect (103), a HSQ dielectric layer (107) and a dielectric layer (109) on top of the HSQ dielectric layer (107), wherein the dielectric layer (109) protects and prevents degradation of the HSQ dielectric layer (107) caused by O_2-containing plasma during photoresist removal (column 3, lines 65-66 and column 4, lines 1-6).

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to provide the claimed sidewalls of the patterned organosilicate dielectric layer not being altered either chemically or physically, as suggested by Wang, in order to provide a low-k dielectric layer without degradation and propensity to absorb moisture from the ambient and where outgassing and voids do not occur when a conductive material is disposed in a through-hole (column 3, lines 22-30).

With regard 2, Gabriel discloses a patterned organosilicate dielectric layer (14) having a dielectric constant of less than 4.0 (column 3, lines 19-24; column 5, lines 64-67 and column 6, lines 1-2).

With regard to Claim 3, Gabriel discloses one or more interconnect levels including metal lines (25) and vias (24); (column 9, lines 32-34).

With regard to Claim 4, Gabriel discloses metal lines (25) and vias (24) comprising a conductive material (column 9, lines 32-34).

With regard to Claim 7, Gabriel discloses one or more device regions that comprise a field effect transistor (column 1, lines 21-36).

3. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gabriel et al. (U.S. Patent No. 6,472,231) in view of Wang et al. (U.S. Patent No. 6,140,706) and further in view of Applicant's admitted prior art as disclosed on page 2 paragraph [0003] of the instant application. With regard to Claims 5 and 6, Gabriel and Wang essentially disclose the claimed invention, but fail to explicitly disclose that the interconnect levels form a thinwire or a fatwire interconnect structure. However, Applicant's admitted prior art discloses that thinwire or fatwire interconnect structures are presently known and formed on integrated circuit chips. Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Gabriel and Wang to include the claimed thinwire or fatwire interconnect structures, as suggested by Applicant's admitted prior art, in order to provide wiring levels fabricated at a minimum lithographic feature size in the case of a thinwire and wiring levels with increased width in the case of a fatwire (see paragraph [0003]).

Response to Arguments

4. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

E.O.
A.U. 2815
5/26/05

GEORGE ECKERT
PRIMARY EXAMINER